

What is claimed is:

- 1 1. A method comprising:
2 translating a design description into configurations for a plurality of
3 processing elements, wherein a plurality of functions in the design description are
4 implemented on one of the plurality of processing elements; and
5 setting at least one output packet size corresponding to at least one of the
6 plurality of functions.
- 1 2. The method of claim 1 wherein setting at least one output packet size
2 comprises setting independent output packet sizes for more than one of the plurality
3 of functions.
- 1 3. The method of claim 1 wherein setting at least one output packet size
2 comprises setting an independent output packet size for each of the plurality of
3 functions.
- 1 4. The method of claim 3 further comprising estimating network performance.
- 1 5. The method of claim 4 further comprising modifying the at least one output
2 packet size and re-estimating network performance.
- 1 6. The method of claim 1 wherein translating comprises compiling the plurality
2 of functions to code to run on the one of the plurality of processing elements.
- 1 7. The method of claim 1 wherein setting a packet size comprises dividing a
2 function output block size into smaller physical block sizes.
- 1 8. The method of claim 7 wherein setting a packet size further includes adding
2 a packet header size to the physical block size.

- 1 9. The method of claim 1 further comprising profiling a design represented by
2 the configurations for the plurality of processing elements.
- 1 10. The method of claim 9 further comprising changing the at least one output
2 packet size in response to the profiling.
- 1 11. The method of claim 9 further comprising comparing user constraints with
2 output from the profiling.
- 1 12. The method of claim 11 wherein the user constraints include latency.
- 1 13. The method of claim 11 wherein the user constraints include throughput.
- 1 14. The method of claim 1 wherein each of the plurality of functions has an
2 output block size, and wherein setting at least one output packet size comprises
3 dividing the output block size to set a physical packet size.
- 1 15. The method of claim 14 wherein setting at least one output packet size
2 further comprises estimating network performance.
- 1 16. The method of claim 15 further comprising changing the physical packet
2 size in response to the estimating.
- 1 17. The method of claim 15 wherein profiling produces information describing
2 throughput.
- 1 18. A method comprising:
2 dividing a design description into a plurality of functions;

3 mapping at least two of the plurality of functions onto one of a plurality of
4 processing elements in an integrated circuit;
5 setting a first output packet size for a first of the at least two of the plurality
6 of functions; and
7 setting a second output packet size for a second of the at least two of the
8 plurality of functions.

1 19. The method of claim 18 wherein the first of the at least two of the plurality
2 of functions has an output block size, and wherein the first output packet size is
3 smaller than the output block size.

1 20. The method of claim 18 further comprising generating configuration packets
2 to configure the integrated circuit.

1 21. The method of claim 20 further comprising configuring the integrated circuit
2 with the configuration packets.

1 22. The method of claim 20 further comprising profiling a design with the
2 configuration packets.

1 23. The method of claim 22 further comprising modifying the first output packet
2 size in response to the profiling.

1 24. An apparatus including a medium to hold machine-accessible instructions
2 that when accessed result in a machine performing:
3 reading a design description;
4 compiling the design description to configure a plurality of processing
5 elements, wherein a plurality of functions in the design description are mapped to
6 one of the plurality of processing elements; and

7 independently determining output packet sizes for each of the plurality of
8 functions.

1 25. The apparatus of claim 24 wherein the machine-accessible instructions when
2 accessed further result in the machine performing:
3 estimating a performance of the plurality of processing elements; and
4 modifying at least one of the output packet sizes in response to the
5 estimating.

1 26. The apparatus of claim 25 wherein estimating a performance comprises
2 determining if throughput constraints are met.

1 27. The apparatus of claim 26 wherein determining if throughput constraints are
2 met comprises determining if throughput constraints for each of the plurality of
3 functions are met.

1 28. An electronic system comprising:
2 a processor; and
3 a static random access memory to hold instructions that when accessed result
4 in the processor performing translating a design description into configurations for a
5 plurality of processing elements on a single integrated circuit, wherein a plurality of
6 functions in the design description are implemented on one of the plurality of
7 processing elements, and setting at least one output packet size corresponding to at
8 least one of the plurality of functions.

1 29. The electronic system of claim 28 wherein setting at least one output packet
2 size comprises setting independent output packet sizes for more than one of the
3 plurality of functions.

1 30. The electronic system of claim 29 wherein setting at least one output packet
2 size comprises setting an independent output packet size for each of the plurality of
3 functions.